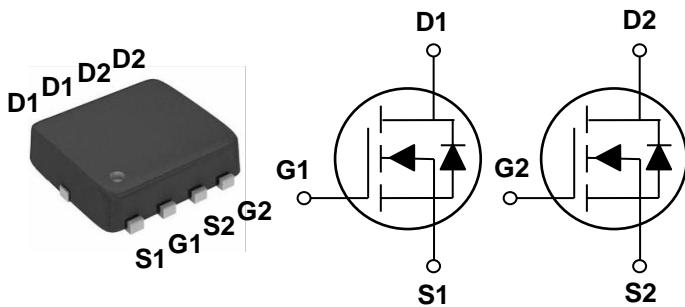


General Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

PPAK3x3 Dual Pin Configuration



BVDSS	RDS(ON)	ID
100V	350mΩ	5.1A

Features

- 100V, 5.1A, RDS(ON) = 350mΩ@VGS = 10V
- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- Green Device Available

Applications

- Networking
- Load Switch
- LED applications



Absolute Maximum Ratings $T_c=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	100	V
V _{Gs}	Gate-Source Voltage	± 20	V
I _D	Drain Current – Continuous ($T_A=25^\circ\text{C}$)	1.6	A
	Drain Current – Continuous ($T_A=70^\circ\text{C}$)	1.28	A
	Drain Current – Continuous ($T_c=25^\circ\text{C}$)	5.1	A
	Drain Current – Continuous ($T_c=100^\circ\text{C}$)	3.2	A
I _{DM}	Drain Current – Pulsed ¹	20.4	A
P _D	Power Dissipation ($T_c=25^\circ\text{C}$)	20.1	W
	Power Dissipation – Derate above 25°C	0.16	W/°C
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction to ambient	---	62	°C/W
R _{θJC}	Thermal Resistance Junction to Case	---	6.2	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)
Off Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	100	---	---	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.09	---	$\text{V}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=100\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{\text{DS}}=80\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=125^\circ\text{C}$	---	---	10	μA
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA

On Characteristics

$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_D=3\text{A}$	---	290	350	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_D=2\text{A}$	---	300	360	$\text{m}\Omega$
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D = 250\mu\text{A}$	1.2	1.8	2.5	V
$\Delta V_{\text{GS(th)}}$	$V_{\text{GS(th)}}$ Temperature Coefficient		---	-5	---	$\text{mV}/^\circ\text{C}$
g_{fs}	Forward Transconductance	$V_{\text{DS}}=10\text{V}$, $I_D=1\text{A}$	---	2.3	---	S

Dynamic Characteristics

Q_g	Total Gate Charge ^{2, 3}	$V_{\text{DS}}=50\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=1\text{A}$	---	9	18	nC
Q_{gs}	Gate-Source Charge ^{2, 3}		---	2.3	4.6	
Q_{gd}	Gate-Drain Charge ^{2, 3}		---	1.1	2.5	
$T_{\text{d(on)}}$	Turn-On Delay Time ^{2, 3}	$V_{\text{DD}}=50\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=3.3\Omega$ $I_D=1\text{A}$	---	5.2	10	ns
T_r	Rise Time ^{2, 3}		---	6.8	12	
$T_{\text{d(off)}}$	Turn-Off Delay Time ^{2, 3}		---	14.5	28	
T_f	Fall Time ^{2, 3}		---	2.1	5	
C_{iss}	Input Capacitance	$V_{\text{DS}}=25\text{V}$, $V_{\text{GS}}=0\text{V}$, $F=1\text{MHz}$	---	492	800	pF
C_{oss}	Output Capacitance		---	27	50	
C_{rss}	Reverse Transfer Capacitance		---	15	25	
R_g	Gate resistance	$V_{\text{GS}}=0\text{V}$, $V_{\text{DS}}=0\text{V}$, $F=1\text{MHz}$	---	2.8	5.6	Ω

Drain-Source Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current	$V_G=V_D=0\text{V}$, Force Current	---	---	5.1	A
I_{SM}	Pulsed Source Current ²		---	---	10.2	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1	V

Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed, pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$.
3. Essentially independent of operating temperature.



STEIF POWER
TECHNOLOGY

100V Dual N-Channel MOSFETs

SPC0854V

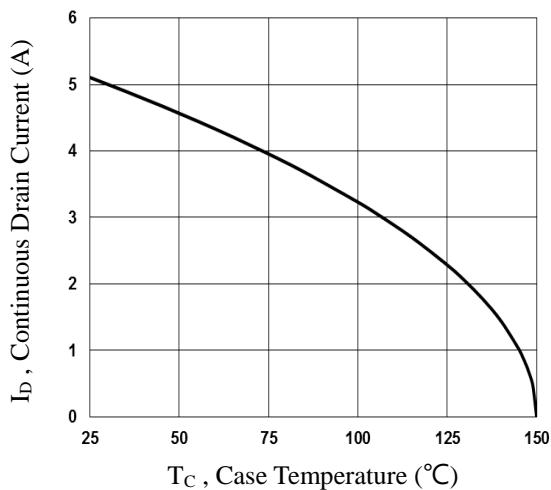


Fig.1 Continuous Drain Current vs. T_c

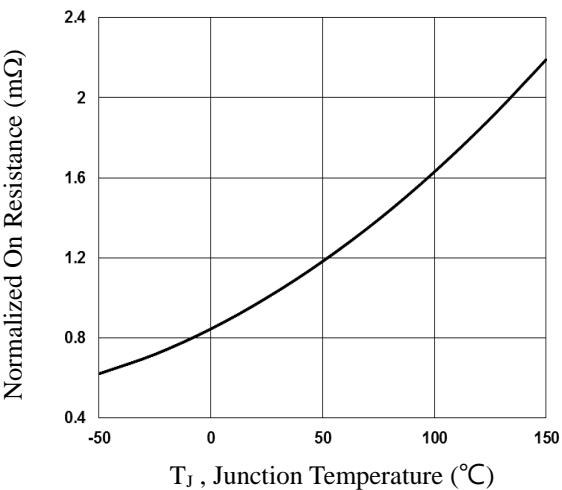


Fig.2 Normalized $R_{DS(on)}$ vs. T_J

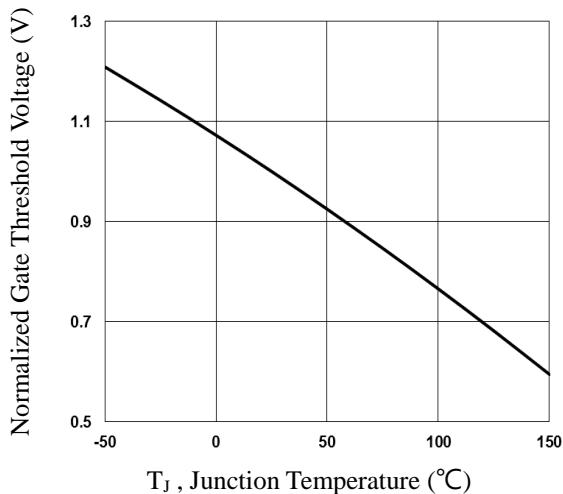


Fig.3 Normalized V_{th} vs. T_J

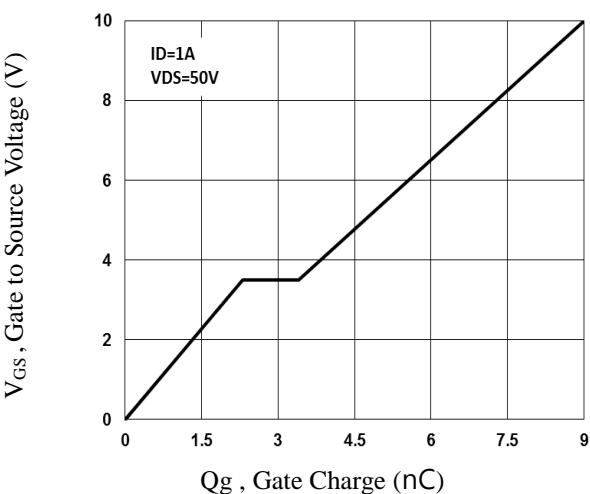


Fig.4 Gate Charge Waveform

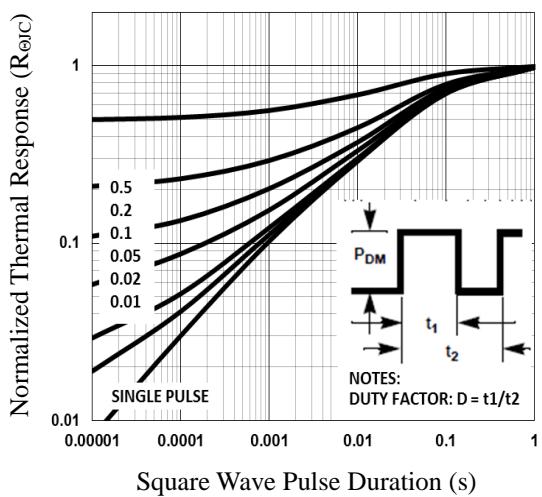


Fig.5 Normalized Transient Impedance

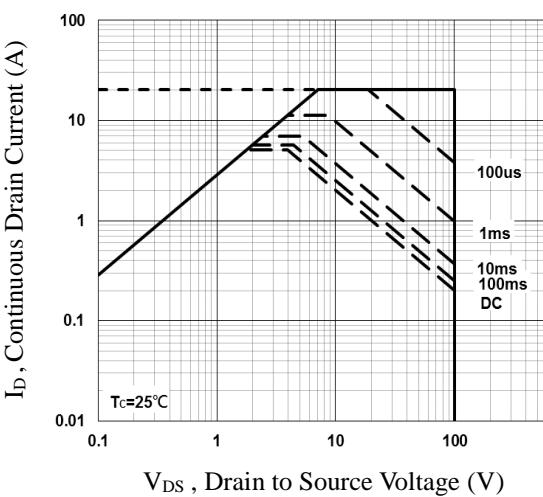


Fig.6 Maximum Safe Operation Area

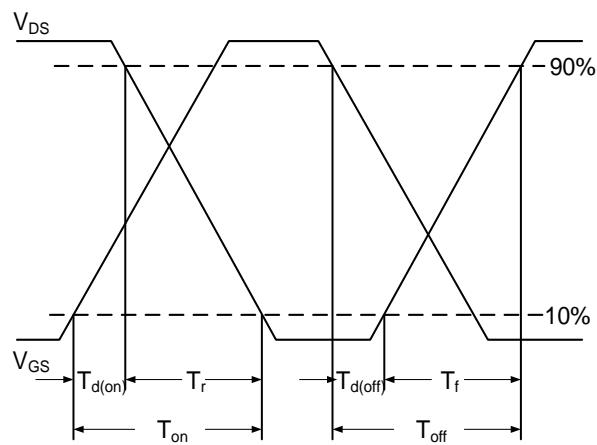


Fig.7 Switching Time Waveform

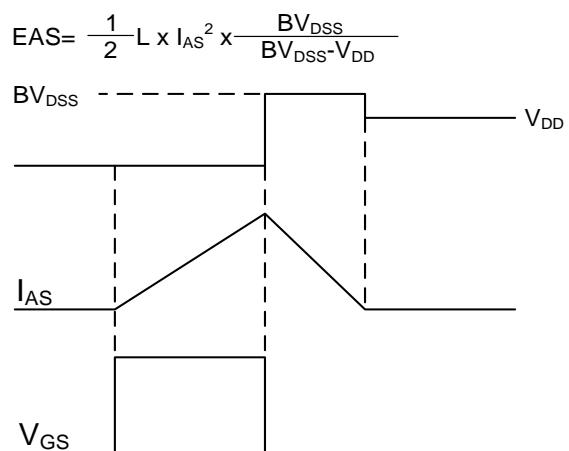
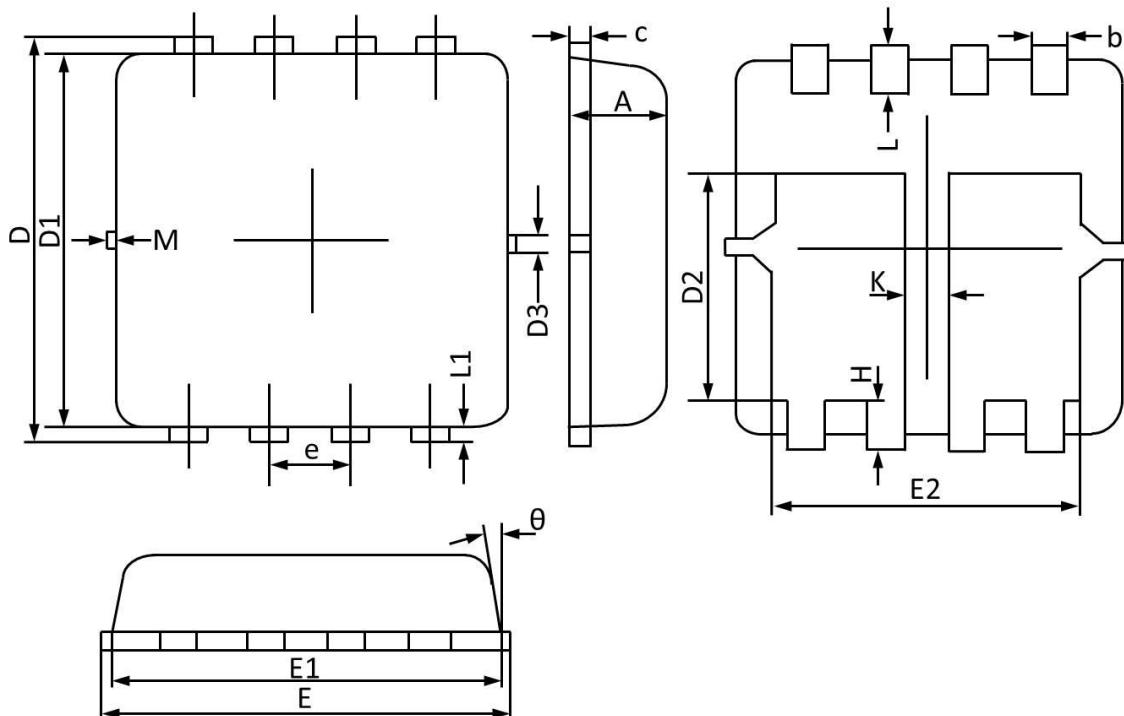


Fig.8 EAS Waveform

**PPAK3x3 Dual PACKAGE INFORMATION**

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
b	0.250	0.350	0.010	0.013
c	0.100	0.250	0.004	0.009
D	3.250	3.450	0.128	0.135
D1	3.000	3.200	0.119	0.125
D2	1.780	1.980	0.070	0.077
D3	0.130 REF		0.005 REF	
E	3.200	3.400	0.126	0.133
E1	3.000	3.200	0.119	0.125
E2	2.390	2.590	0.094	0.102
e	0.650 BSC		0.026 BSC	
H	0.300	0.500	0.011	0.019
L	0.300	0.500	0.011	0.019
L1	0.130 REF		0.005 REF	
K	0.300 REF		0.012 REF	
θ	0°	12°	0°	12°
M	0.150 REF		0.006 REF	